IN THE CLAIMS:

Please cancel claims 1-20 and add new claims 46 to 63 as indicated on the following listing of all the claims in the present application after this Amendment. Claims 21-45 were cancelled in the Preliminary Amendment.

1-45 Cancelled

46. (New) A method of programming cells of a memory array in which cell threshold voltages represent logical states, comprising:

programming a plurality of cells that are to be programmed to a first threshold voltage or higher to the first threshold voltage and inhibiting individual cells of the plurality that reach the first threshold voltage until all cells of the plurality are at the first threshold voltage;

subsequently further programming individual cells of the plurality of cells that are to be programmed to a second threshold voltage or higher by inhibiting individual cells that reach the second threshold voltage until all cells that are to be programmed to the second threshold voltage or higher reach the second voltage; and

subsequently further programming individual cells of the plurality of cells that are to be programmed to a third threshold voltage or higher.

47. (New) The method of claim 46 wherein further programming individual cells of the plurality of cells that are to be programmed to a third threshold voltage or higher includes programming individual cells to the third, a fourth and higher threshold voltage levels with cells being inhibited at the third, fourth and each higher threshold voltage until each of the plurality of cells has reached its target threshold level.

48. (New) The method of claim 46 wherein a threshold voltage is determined by the charge stored in a floating gate of a cell.

49. (New) The method of claim 48 wherein in an unprogrammed state the floating gate has no charge and the cell has a fourth threshold voltage.

50. (New) The method of claim 49 wherein the first threshold voltage represents a first logical state, the second threshold voltage represents a second logical state, the third threshold voltage represents a third logical state and the fourth threshold voltage represents a fourth logical state.

51. (New) The method of claim 50 wherein the first and fourth logical states represent a bit of data of a first page and the second and third logical states represent a bit of data of a second logical page.

52. (New) The method of claim 46 wherein programming includes applying an electrical pulse to a memory cell and verifying the threshold voltage of the cell one or more times.

53. (New) A method of programming floating gates of a memory array to charge levels that correspond to logical states, comprising:

charging a first, a second and a third floating gate together to a first charge level by inhibiting a floating gate that reaches the first charge level until the first, second and third floating gates are all at the first charge level;

subsequently charging the second and the third floating gates to a second charge level by inhibiting a floating gate that reaches the second charge level until the second and third floating gates are both at the second charge level;

subsequently charging the third floating gate to the third charge level.

54. (New) The method of claim 53 further comprising inhibiting charging of the first floating gate once the first floating gate reaches the first charge level.

55. (New) The method of claim 53 further comprising inhibiting charging of the second floating gate once the second floating gate reaches the second charge level.

56. (New) The method of claim 53 further comprising inhibiting a fourth floating gate in an unprogrammed condition while charging the first, second and third floating gates.

57. (New) The method of claim 53 further comprising charging a fourth floating gate from an unprogrammed condition to the second charge level simultaneously with programming the first floating gate from the first charge level to the second charge level.

58. (New) A memory device that stores data in cells of a memory array where the threshold voltages of cells signify logical states, comprising:

a first plurality of memory cells to be programmed to a first threshold voltage;

a second plurality of memory cells to be programmed to a second threshold voltage;

a third plurality of memory cells to be programmed to a third voltage; and

a programming circuit that programs the first, second and third pluralities of cells to the first threshold voltage and inhibits programming of individual ones of the first, second and third pluralities of cells that reach the first threshold voltage until all cells of the first, second and third pluralities of cells reach the first threshold voltage and subsequently further programs the second and third pluralities of cells to the second threshold voltage and inhibits programming of individual ones of the second and third pluralities of cells that reach the second threshold voltage until all cells of the second and third pluralities reach the second threshold voltage and subsequently further programs the third plurality of cells to the third threshold voltage.

59. (New) The memory device of claim 58 further comprising an interface that connects the memory device to a socket in a host.

60. (New) The memory device of claim 58 wherein the memory array comprises a plurality of strings of memory cells, a string having select gates.

61. (New) The memory device of claim 58 wherein the memory array is a NAND flash memory array.

62. (New) The memory device of claim 58 wherein the memory array is formed on a first integrated circuit chip and the programming circuit is formed on a second integrated circuit chip.

63. (New) The memory device of claim 58 wherein the first, second and third pluralities of memory cells are connected by a common wordline.